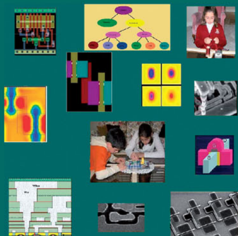
Charles Chiang
Jamil Kawa



Design for Manufacturability and Yield for Nano-Scale CMOS

Springer

DESIGN FOR MANUFACTURABILITY AND YIELD
FOR NANO-SCALE CMOS

Series on Integrated Circuits and Systems

Series Editor: Anantha Chandrakasan
Massachusetts Institute of Technology
Cambridge, Massachusetts

Low Power Methodology Manual: For System-on-Chip Design
Michael Keating, David Flynn, Rob Aitken, Alan Gibbons, and Kaijian Shi
ISBN 978-0-387-71818-7

Modern Circuit Placement: Best Practices and Results
Gi-Joon Nam and Jason Cong
ISBN 978-0-387-36837-5

CMOS Biotechnology
Hakho Lee, Donhee Ham and Robert M. Westervelt
ISBN 978-0-387-36836-8

SAT-Based Scalable Formal Verification Solutions
Malay Ganai and Aarti Gupta
ISBN 978-0-387-69166-4, 2007

Ultra-Low Voltage Nano-Scale Memories
Kiyoo Itoh, Masashi Horiguchi and Hitoshi Tanaka
ISBN 978-0-387-33398-4, 2007

Routing Congestion in VLSI Circuits: Estimation and Optimization
Prashant Saxena, Rupesh S. Shelar, Sachin Sapatnekar
ISBN 978-0-387-30037-5, 2007

Ultra-Low Power Wireless Technologies for Sensor Networks
Brian Otis and Jan Rabaey
ISBN 978-0-387-30930-9, 2007

Sub-Threshold Design for Ultra Low-Power Systems
Alice Wang, Benton H. Calhoun and Anantha Chandrakasan
ISBN 978-0-387-33515-5, 2006

High Performance Energy Efficient Microprocessor Design
Vojin Oklibdzija and Ram Krishnamurthy (Eds.)
ISBN 978-0-387-28594-8, 2006

Abstraction Refinement for Large Scale Model Checking
Chao Wang, Gary D. Hachtel, and Fabio Somenzi
ISBN 978-0-387-28594-2, 2006

A Practical Introduction to PSL
Cindy Eisner and Dana Fisman
ISBN 978-0-387-35313-5, 2006

Thermal and Power Management of Integrated Systems
Arman Vassighi and Manoj Sachdev
ISBN 978-0-387-25762-4, 2006

Leakage in Nanometer CMOS Technologies
Siva G. Narendra and Anantha Chandrakasan
ISBN 978-0-387-25737-2, 2005

Statistical Analysis and Optimization for VLSI: Timing and Power
Ashish Srivastava, Dennis Sylvester, and David Blaauw
ISBN 978-0-387-26049-9, 2005

DESIGN FOR MANUFACTURABILITY AND YIELD FOR NANO-SCALE CMOS

by

CHARLES C. CHIANG

Synopsys Inc.
Mountain View, CA, USA

and

JAMIL KAWA

Synopsys Inc.
Mountain View, CA, USA

Springer

A C.I.P. Catalogue record for this book is available from the Library of Congress.

ISBN 978-1-4020-5187-6 (HB)
ISBN 978-1-4020-5188-3 (e-book)

Published by Springer,
P.O. Box 17, 3300 AA Dordrecht, The Netherlands.

www.springer.com

Printed on acid-free paper

The contributing authors of this book have used figures and content published in IEEE conferences and journals (© IEEE). Those figures and content from IEEE publications that are included in this book are printed with permission from the IEEE

All Rights Reserved
© 2007 Springer
No part of this work may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electronic, mechanical, photocopying, microfilming, recording or otherwise, without written permission from the Publisher, with the exception of any material supplied specifically for the purpose of being entered and executed on a computer system, for exclusive use by the purchaser of the work.

To my wife Susan
(Show-Hsing) and my
daughters Wei Diana and
Ann - Charles

To my wife Zeina and my
children Nura, Tamara,
and Rami - Jamil

Contents

List of Figures xiii

List of Tables xix

Preface xxi

Acknowledgments xxvii

1. INTRODUCTION 1

  1.1 What is DFM/DFY 1

  1.2 DFM/DFY Critical for IC Manufacturing 2

    1.2.1 New Materials 3

    1.2.2 Sub-wavelength Lithography 6

    1.2.3 New Devices 9

    1.2.4 Proliferation of Processes 12

    1.2.5 Intra-die Variability 14

    1.2.6 Error Free Masks Too Costly 15

    1.2.7 Cost of a Silicon Spin 15

  1.3 DFM Categories and Classifications 16

    1.3.1 First Time Failures 16

    1.3.2 Time Related Failures 17

  1.4 How Do Various DFM Solutions Tie up with Specific Design Flows 17

  1.5 DFM and DFY: Fully Intertwined 19

2. RANDOM DEFECTS 21

  2.1 Types of Defects 21

  2.2 Concept of Critical Area 22

2.3 Basic Models of Yield for Random Defects 23
2.4 Critical Area Analysis (CAA) 24
2.4.1 Classical Methods of CA Extraction 24
2.4.2 Approximations 25
2.4.3 Comparison of Approximate and Traditional CA 26
2.5 Mathematical Formulation of Approximation Method 26
2.5.1 Short Critical Area - Mathematical Formulation 27
2.5.2 Open Critical Area - Mathematical Formulation 31
2.6 Improving Critical Area 34
2.6.1 Cell Library Yield Grading 34
2.6.2 Average CA Yield Improvement 36
2.6.3 Weighted Average CA Yield Improvement 41
2.6.4 Key Benefits of the Proposed Algorithm 47
2.7 Experimental Results 48
2.7.1 Validation of Fast Critical Area Analysis Evaluation 48
2.7.2 Comparison of Critical Area Reductions 48
2.7.3 Discussion 50
2.8 Conclusions 51
3. SYSTEMATIC YIELD - LITHOGRAPHY 53
3.1 Introduction 53
3.2 Optics Fundamentals 53
3.3 Basic Design Flow 55
3.4 Lithography and Process Issues 57
3.4.1 Masks Writing 57
3.4.2 Optical System Interactions 57
3.4.3 Resist 57
3.4.4 Etch 58
3.5 Resolution Enhancement Technique (RET) 58
3.5.1 Optical Proximity Correction (OPC) 59
3.5.2 Sub Resolution Assist Feature (SRAF) 63
3.5.3 Phase Shift Masks (PSM) 65
3.5.4 Off Axis Illumination (OAI) 71
3.6 Other Optical Techniques 73
3.6.1 Immersion Technology 73
3.6.2 Double Dipole Lithography (DDL) 73

3.6.3 Chromeless Phase Lithography (CPL) 74

3.7 Lithography Aware Routing 74

3.8 RET and Lithography Verification 75

3.8.1 Lithography Rule Check (LRC) 76

3.8.2 Pattern Simulation 77

3.9 Integrated Flow 77

3.9.1 Mask Preparation and Repair 77

3.9.2 Design Intent 79

3.9.3 Silicon vs. Layout 80

3.10 Yield Considerations 81

3.10.1 Cell Design Considerations 81

3.10.2 Yield Optimized Routing 82

3.11 Practical Application 83

3.11.1 Framing the problem 83

3.11.2 Potential Solutions 84

3.11.3 Proposed Solution 84

3.11.4 Framing the Solution - Definitions and Presentation 85

3.11.5 Litho-Hotspot Detection System 88

3.11.6 Summary & Results 95

3.12 DFM & DFY Centric Summary 96

3.13 Lithography Specific Summary 97

4. SYSTEMATIC YIELD - CHEMICAL MECHANICAL POLISHING (CMP) 99

4.1 Introduction 99

4.2 The Dual Damascene Process 100

4.2.1 Via-first Dual-Damascene Process 101

4.2.2 The Dielectric 101

4.2.3 The Metal Barrier 101

4.3 Electroplating 102

4.3.1 Procedure Description 102

4.3.2 Electroplating Model 105

4.4 A Full Chip Simulation Algorithm 112

4.4.1 Case Selection 113

4.4.2 Tile Size and Interaction Length 115

4.4.3 Model Verification 116

4.4.4 Key Advantages of ECP Topography Model 121

4.5 CMP 121

4.5.1 CMP Process Description 122

4.6 Dummy Filling 124

4.6.1 Rule Based 125

4.6.2 Model Based 125

4.7 Application: ILD CMP Model Based Dummy Filling 127

4.7.1 Introduction 127

4.7.2 The 2-D Low-pass-filter CMP Model 128

4.7.3 The Dummy Filling Problem 128

4.7.4 The Linear Programming Method 129

4.7.5 The Min-variance Interactive Method 129

4.7.6 Improving the Detection Capability 132

4.7.7 Simulation Results 134

4.8 Application: Cu CMP Model Based Dummy Filling 139

4.8.1 Why Model Based Metal Filling? 139

4.8.2 Predictors of the Final (Post-CMP) Thickness Range 140

4.8.3 ECP Thickness Versus Final Thickness 141

4.8.4 Effective Density Versus Final Thickness 141

4.8.5 Details of the Proposed Metal Filling Algorithm 142

4.8.6 Experimental Results 148

4.8.7 Discussion of Results 148

5. VARIABILITY & PARAMETRIC YIELD 151

5.1 Introduction to Variability and Parametric Yield 151

5.2 Nature of Variability 151

5.3 Source of Variability 152

5.3.1 Wafer Level Variability 153

5.3.2 Materials Based Variability 155

5.3.3 Atomistic Variability 157

5.3.4 Lithography Based Variability 157

5.3.5 Local Variability 159

5.3.6 Environmental Variability & Aging 159

5.3.7 Device and Interconnect Parameters Variability 162

5.4 Yield Loss Sources & Mechanisms 164

5.5 Parametric Yield 166